

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A pixel cell comprising:

a photosensor;

a charge collection region coupled to said photosensor for receiving charge generated by said photosensor; and

at least two storage capacitors coupled in series with each other, said series-connected capacitors also being coupled in series with said charge collection region for receiving charge from said charge collection region.
2. The pixel cell of claim 1, wherein at least one of said at least two storage capacitors is a flat plate capacitor.
3. The pixel cell of claim 1, wherein at least one of said at least two storage capacitors is a trench capacitor.
4. The pixel cell of claim 1, wherein at least one of said at least two storage capacitors is a stud capacitor.
5. The pixel cell of claim 1, wherein said photosensor is a photodiode.
6. The pixel cell of claim 1, wherein said photosensor is a photogate.
7. The pixel cell of claim 1, wherein the charge collection region is a floating diffusion region.

8. The pixel cell of claim 1, further comprising a transfer transistor gate formed between said photosensor and said charge collection region.

9. A pixel cell comprising:

a photosensor;

a charge collection region coupled to said photosensor for receiving charge generated by said photosensor; and

an array capacitance formed of at least two series-connected storage capacitors coupled to said charge collection region, said array capacitance having a capacitance value lower than that of a periphery capacitance switchably coupled to said pixel cell.

10. The pixel cell of claim 9, wherein said at least two series-connected storage capacitors are coupled between said charge collection region and a voltage source terminal.

11. The pixel cell of claim 10, wherein said voltage source terminal is a V_{dd} terminal.

12. The pixel cell of claim 9, wherein said at least two storage capacitors are formed adjacent to one another at substantially the same level above said charge collection region.

13. The pixel cell of claim 9, wherein the charge collection region is a floating diffusion region.

14. The pixel cell of claim 9, further comprising a transfer transistor formed between said photosensor and said charge collection region.

15. A semiconductor chip containing a CMOS imager including an array of pixels, each pixel cell of said array comprising:

a photosensor;

a charge collection region coupled to said photosensor for receiving charge generated by said photosensor; and

an array capacitance formed of at least two series-connected storage capacitors coupled to said charge collection region, said array capacitance having a capacitance value lower than that of a periphery capacitance located outside said pixel array.

16. An imager integrated circuit comprising:

an array of pixel cells formed in a semiconductor substrate, wherein each pixel cell of said array comprises:

a photosensor;

a charge collection region coupled to said photosensor for receiving charge generated by said photosensor;

at least two storage capacitors coupled in series with each other, said series-connected capacitors also being coupled in series with said charge collection region for receiving charge from said charge collection region; and

signal processing circuitry formed in said substrate and electrically connected to the array for receiving and processing pixel signals representing

an image acquired by the array and for providing output data representing said image.

17. A processing system comprising:

a processor;

an imaging device coupled to said processor, said imaging device having a plurality of pixel cells, at least one of said pixel cells comprising:

a photosensor;

a charge collection region coupled to said photosensor for receiving charge generated by said photosensor; and

at least two storage capacitors coupled in series with each other, said series-connected capacitors also being coupled in series with said charge collection region for receiving charge from said charge collection region.

18. A method of forming a pixel cell, the method comprising:

forming a photosensor;

forming a charge collection region coupled to said photosensor; and

forming at least two storage capacitors coupled in series with each other, said series-connected capacitors also being coupled in series with said charge collection region for receiving charge from said charge collection region.

19. The method of claim 18, wherein said act of forming at least two storage capacitors comprises forming at least one flat plate capacitor.

20. The method of claim 18, wherein said act of forming at least two storage capacitors comprises forming at least one trench capacitor.

21. The method of claim 18, wherein said act of forming at least two storage capacitors comprises forming at least one stud capacitor.

22. The method of claim 18, wherein said act of forming a photosensor comprises forming a photodiode.

23. The method of claim 18, wherein said act of forming a photosensor comprises forming a photogate.

24. The method of claim 18, further comprising forming a transfer transistor between said photosensor and said first charge collection region.

25. A method of forming a CMOS imager including an array of pixels, at least one pixel cell of said array formed by:

forming a charge collection region within a substrate;

forming at least one periphery capacitor coupled to said pixel cell; and

forming at least two series-connected storage capacitors within said pixel cell at substantially the same time as said act of forming said at least one periphery capacitor.

26. The method of claim 25, wherein said act of forming said at least two series-connected storage capacitor comprises forming a said at least two series-connected storage capacitors above said charge collection region.

27. The method of claim 25, wherein said act of forming charge collection region comprises forming a floating diffusion region.

28. The method of claim 25, wherein said act of forming at least two series-connected capacitors comprises forming said at least two capacitors at substantially the same level above said charge collection region.